This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on a surface of the chip carrier and electrically connected to the chip carrier;

a heat sink having a first surface, a second surface opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the chip for interposing the chip between the chip carrier and the heat sink;

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an interface layer formed on the second surface of the heat sink, and made of a material having adhesion with a molding compound smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and

an encapsulant made of the molding compound for encapsulating the chip, the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, the side surfaces of the heat sink are flush with side edges of the encapsulant, and the molding compound left on the interface layer during formation of the encapsulant is easily and thermally removable from the interface layer, so as to make the semiconductor package free of flash of the molding compound because of the relatively smaller adhesion between the interface layer and the molding compound and a difference in thermal expansion coefficient between the interface layer and the molding compound.

Claim 2 (original): The semiconductor package of claim 1, wherein the heat sink has a surface area dimensionally same as that of the chip carrier.

Claim 3 (previously presented): The semiconductor package of claim 1, wherein the material for making the interface layer on the second surface of the heat sink is selected from the group

consisting of gold, chromium, nickel, alloy thereof and Teflon (polytetrafluoroethylene).

Claim 4 (original): The semiconductor package of claim 1, wherein the chip carrier is a substrate.

Claim 5 (original): The semiconductor package of claim 4, wherein the chip is electrically connected to the substrate through bonding wires.

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Claim 6 (original): The semiconductor package of claim 4, wherein the chip is electrically connected to the substrate through solder bumps.

Claim 7 (original): The semiconductor package of claim 1, wherein the chip carrier is a QFN (quad flat nonlead) lead frame.

Claim 8 (original): The semiconductor package of claim 7, wherein the chip is electrically connected to the QFN lead frame through bonding wires.

Claim 9 (original): The semiconductor package of claim 1, wherein the first surface of the heat sink is roughened, corrugated or made uneven.

Claim 10 (previously presented): The semiconductor package of claim 1, wherein at a position on the first surface of the heat sink corresponding to the chip there is formed a connecting portion extending toward the chip for connecting the heat sink to the chip through the connecting portion, and the first surface of the heat sink other than the position of the connecting portion is spaced apart from the chip.

Claims 11-20 (canceled)

Claim 21 (new): The semiconductor package of claim 1, wherein a buffer pad is interposed between the chip and the heat sink, and made of a material having a similar thermal expansion coefficient to the chip.

Claim 22 (new): The semiconductor package of claim 1, further comprising a plurality of solder balls implanted on a surface of the chip carrier opposite to the surface mounted with the chip.

Claim 23 (new): A fabrication method of a semiconductor package with a heat sink, comprising the steps of:

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preparing a chip carrier module plate formed of a plurality of chip carriers each having an upper surface and an opposite lower surface;

mounting at least one chip on the upper surface of each of the chip carriers and electrically connecting the chip to the corresponding chip carrier;

preparing a heat sink module plate formed of a plurality of heat sinks and having a first surface and an opposite second surface, attaching the first surface of the heat sink module plate to the chips, and forming an interface layer over the second surface of the heat sink module plate, wherein the interface layer is made of a material having adhesion with a molding compound smaller than adhesion between the heat sinks and the molding compound;

forming an encapsulant by the molding compound for encapsulating the chip, the heat sink module plate, and the chip carrier module plate;

implanting a plurality of solder balls on the lower surface of the chip carrier module plate;

performing a singulation process to cut through the interface layer, the heat sink module plate, the encapsulant, and the chip carrier module plate to separate apart the plurality of heat sinks and chip carriers so as to form a plurality of the semiconductor packages; and

removing the molding compound left on the interface layer by heating due to the relatively smaller adhesion between the interface layer and the molding compound and a difference in thermal expansion coefficient between the interface layer and the molding compound, so as to make the semiconductor packages free of flash of the molding compound.

Claim 24 (new): The fabrication method of claim 23, wherein a buffer pad is interposed between the chip and the heat sink, and made of a material having a similar thermal expansion coefficient to the chip.

Claim 25 (new): The fabrication method of claim 23, wherein the material for making the interface layer is selected from the group consisting of gold, chromium, nickel, alloy thereof and Teflon (polytetrafluoroethylene).

Claim 26 (new): The fabrication method of claim 23, wherein the chip carrier is a substrate.

Claim 27 (new): The fabrication method of claim 26, wherein the chip is electrically connected to the substrate through bonding wires.

Claim 28 (new): The fabrication method of claim 23, wherein the chip carrier is a QFN (quad flat nonlead) lead frame.

Claim 29 (new): The fabrication method of claim 28, wherein the chip is electrically connected to the QFN lead frame through bonding wires.

Claim 30 (new): The fabrication method of claim 23, wherein the first surface of the heat sink module plate is roughened, corrugated or made uneven.